1. A low capacitance depletion mode SCR and NFET element integrated circuit semiconductor device structure with associated parasitic bipolar transistors on a substrate for the purpose of providing electrostatic voltage discharge protection to the active semiconductor devices comprising:

a first doped region of opposite dopent than said substrate;

a second doped region within said first doped region of opposite dopent than said second doped region;

a plurality of third doped regions within said substrate of opposite dopent than said substrate

a gate structure overlaying said substrate surface between a first element and second element of said third doped regions;

a gate structure overlaying said substrate surface between a third element and fourth element of said third doped regions;

a first isolation element between said second element of said third doped region and a first side of said second doped region;

a second isolation element between said third element of said third doped regions and a second side of said second doped region;

a plurality of fourth doped regions within said substrate of similar dopent as said substrate;

an electrical connection system for said second doped region;

an electrical connection system for said first and fourth elements of said third doped regions and for the first and second elements of said fourth doped regions;

a surface passivation layer for said ESD protection device.

2. The structure according to claim 1 wherein said substrate consists of silicon semiconductor

material doped to a concentration between 1E15 and 1E16 a/cm$^3$.

3. The structure according to claim 1 wherein said first doped region is doped with a donor element such as As to a concentration between 5E15 to 1E18 a/cm$^3$ and has a width between 0.5 to 6 um and a depth between 0.5 and 6 um to form a N-well.

4. The structure according to claim 1 wherein said second doped region is doped with an acceptor element such as boron to a concentration between 1E19 and 1E21 a/cm$^3$ to form a N-well P+ contact region.

5. The structure according to claim 1 wherein said plurality of third doped regions are doped with an acceptor element such as arsenic to a concentration of between 1E19 and 1E21 a/cm$^3$.

6. The structure according to claim 1 wherein said first and fourth elements of said third doped regions form the N+ drain regions of NFET elements.

7. The structure according to claim 1 wherein said second and third elements of said third doped regions form the drain regions of said NFET elements and are electrically floating.

8. The structure according to claim 1 wherein said gate elements are comprised of gate oxide to a thickness between 50 and 300 Å. and polysilicon to a thickness between 3000 and 6000 Å.

9. The structure according to claim 1 wherein said polysilicon is doped with a donor element to a concentration between 1E19 and 1E21 a/cm$^3$.

10. The structure according to claim 1 wherein said isolation elements consist of shallow trench isolation structures with a width of between 0.1 and 3 um and a depth of between 0.5 and 4 um.

11. The structure according to claim 1 wherein said isolation elements are filled with a first layer of $SiO_2$ to a thickness of between 50 and 500Å and then filled with a second layer of $SiO_2$ to said substrate surface.

12. The structure according to claim 1 wherein said plurality of fourth dope regions are doped

with an acceptor dopent such as boron to a concentration between 1E19 and 1E21 a/cm$^3$ to form P+ contact elements for said substrate.

13. The structure according to claim 1 wherein said electrical connection system for said second doped region consists of aluminum metallurgy or aluminum doped with 1 % silicon metallurgy, and is connected to a first voltage source consisting of the input pad of said active semiconductor devices.

14. The structure according to claim 1 wherein said electrical connection system for said first and fourth elements of said third doped regions and for the first and second elements of said fourth doped regions consists of aluminum metallurgy or aluminum doped with 1 % silicon metallurgy, and is connected to a second voltage source or ground.

15. The structure according to claim 1 wherein said surface passivation layer for said ESD protection device consists of deposited $SiO_2$ doped with boron and phosphorous to form BPSG.

16. A method of forming a low input capacitance depletion mode SCR and isolated N channel FET ESD protection device on a semiconductor substrate comprising:

creating a N-well within said semiconductor substrate;

creating multiple STI structures within said substrate bridging said N-well and said substrate boundary in the surface region;

creating gate elements on said substrate surface;

creating N+ source and drain areas within said substrate on either side of said gate elements forming NFET elements;

creating a P+ contact region within said N-well region and creating P+ contact regions within said substrate outside of said N-well region;

creating a first and second electrical conductor system for said ESD protection device;

creating passivation for said ESD protection device.

17. The method according to claim 16 whereby said gate elements are comprised of a thin $SiO_2$ insulation layer and a polysilicon conductor element.

18. The method according to claim 16 whereby said P+ N-well contact region is connected to the active circuit signal input pad by said first electrical conductor system.

19. The method according to claim 16 whereby said gate elements and said NFET N+ source elements are electrically floating.

20. The method according to claim 16 whereby said NFET N+ source elements and said substrate P+ contact elements are connected to ground by said second electrical conductor system.

21. The method according to claim 16 whereby said conductor system is comprised of a metallurgy such as aluminum or aluminum doped with silicon.

22. The method according to claim 16 whereby said passivation is a silicon glass such as borophosphorus silicate glass.

23. A method of fabricating a low input capacitance depletion mode SCR and isolated N channel FET semiconductor device with associated parasitic bipolar transistors to provide ESD protection on a semiconductor substrate comprising:

Growing a first layer on said substrate surface;

depositing a second layer on surface of said first layer;

defining with a first patterning element a region for a first doped region;

Etching said first and said second surface layers for said first doped region;

implanting a dopent to form said first doped region;

reestablishing said surface layers;

defining with a second patterning element regions for isolation elements;

etching said surface layers and said substrate creating open shallow trenches for said isolation elements;

forming a protective covering on open walls of said open shallow trenches;

filling and capping and planarizing said shallow trench isolation elements;

replacing said first and second surface layers with a third surface layer;

depositing a conductive layer on said third surface layer;

defining with a third patterning element plurality of regions for a third doped region;

implanting said third regions with a donor element;

patterning with a fourth patterning element for a plurality of fourth doped regions;

implanting said fourth doped regions with an acceptor dopent;

forming a conductor system for said protection device;

forming a passivation layer for said protection device;

completing the processing of said protection device.

24. The method according to claim 23 wherein said substrate is doped with a donor element such as phosphorous to provide a P doping density of between 1E15 and 1 E16 a/cm$^3$.

25. The method according to claim 23 wherein said first surface layer is thermally grown $SiO_2$ to a thickness of between 70 and 600Å.

26. The method according to claim 23 wherein said second surface layer is SiN deposited by LPCVD to a thickness between 800 and 2000A.

27. The method according to claim 23 wherein said first doped region is formed with an ion implant of phosphorous (P) with an energy level between 30 and 100 KeV and a dosage level between 1E11 and 1E14 a/cm$^2$ to produce a N-well region with a concentration between 5E15

and 1E18 a/cm$^3$.

28. The method according to claim 23 wherein said shallow trench isolation elements are anisotropically etched by reactive ion etching to a width of between 0.1 and 3 um wide and between 0.5 and 4 um deep.

29. The method according to claim 23 wherein said protective coating on said open walls of said open shallow trenches consists of thermal deposited $SiO_2$ to a thickness of between 50 and 500 Å.

30. The method according to claim 23 wherein said shallow trench elements are filled and capped with thermally grown $SiO_2$.

31. The method according to claim 23 wherein said filled shallow trench isolation elements are planarized by chemical mechanical polishing.

32. The method according to claim 23 wherein said third surface layer is thermally deposited $SiO_2$ for gate insulator to a thickness between 50 and 300 Å.

33.The method according to claim 23 wherein said first conducting layer is polysilicon provided by low pressure chemical vapor deposition at a temperature between 550 and 700 °C using a silane source or a gas with hydrogen or nitrogen.

34. The method according to claim 23 wherein said third doped regions are doped with phosphorous (P) with an energy level between10 and 80 KeV and a dosage level between 1E14and 1E17 a/cm$^2$ to produce N+ source drain areas with a dopent concentration of between E19 and E21 a/cm$^3$.

35. The method according to claim 23 wherein said fourth doped regions are doped with boron with an energy level between 10 and 80 KeV and with a dosage level between 1E14and 1E17 a/cm$^2$ to produce said substrate P+ contact regions with a concentration of between E19 and E21

$a/cm^3$.

36. The method according to claim 23 wherein said conductor system is made by a blanket evaporation of aluminum doped with 1% silicon, followed by a RIE etched to remove unwanted metal.

37. The method according to claim 23 wherein said passivation layer consists of silicon oxide doped with boron and phosphorous to form borophosphorus silicate glass and is thermally deposited at a temperature between 400 and 500 °C.